Remarks

In the Office Action dated January 26, 2005, the Examiner rejected 23-26 under 35 U.S.C. § 103(a) as being unpatentable over *Snider* (U.S. Patent No. 5,991,893) in view of *Nikhil et al.* (U.S. Patent No. 5,499,349) and rejected claims 30-34 under 35 U.S.C. § 103(a) as being unpatentable over *Resman et al.* (U.S. Patent No. 5,535,364) in view of *Nikhil et al.*

Based on the following remarks, Applicant respectfully traverses the rejection of claims 23-26 and 30-34 under 35 U.S.C. § 103(a).

I. The Information Disclosure Statements Filed January 14, [*sic*] 2003 and October 10,[*sic*] 2004

Applicant appreciates the Examiner's acknowledgement of the Information Disclosure Statements (IDSs) filed January 28, 2005 and April 6, 2005. Unfortunately, the Examiner refuses to acknowledge and consider the references attached to the IDSs filed January 14, [*sic*] 2003 and October 10, [*sic*] 2004. The Examiner's refusal is improper. It is long standing practice for an applicant to show proof of receipt of correspondence to the USPTO via the stamped postcard accompanying the correspondence. Indeed, 37 C.F.R. § 1.6 and M.P.E.P. § 505 acknowledges "[c]orrespondence received in the Patent and Trademark Office is stamped with the date of receipt." Accordingly, for an applicant to have the Examiner consider any timely filed correspondence that is missing from the USPTO's application file, the applicant need only provide proof of receipt by the USPTO and possibly a copy of the correspondence. Commonly, this is done via the stamped post card that accompanies the filed correspondence, which Applicant has done. Applicant has provided, and the Examiner acknowledges receipt of, copies of the IDSs filed January 15, 2003 and

October 29, 2004 that Applicant submitted again with the Response filed April 4, 2005. (OA at 3, ¶ 3.) As noted in the Amendment, copies of the stamped postcards showing receipt by the USPTO of these filed IDSs was also provided to the Examiner. (*See* Response filed 4/4/05 at 2.) As such, it is improper for the Examiner to refuse to consider these IDSs merely because copies of the IDSs are not found in the USPTO's file wrapper. As a courtesy, Applicant submits for the third time copies of the IDSs filed January 15, 2003 and October 29, 2004 and each corresponding stamped postcard showing receipt by the U.S. Patent and Trademark Office. In this regard, Applicant again requests that the Examiner provide copies of initialed PTO Form 1449s associated with these IDSs indicating that the references listed therein have been considered by the Examiner.

II. The Rejection of Claims 23-26

The Examiner maintains the same rejections of claims 23-26 under 35 U.S.C. § 103(a) over *Snider* in view of *Nikhil et al.* set forth in the previous office action mailed January 26, 2005. The Examiner, however, supplements this rejection with comments addressing the arguments presented by Applicant in the April 4, 2005 Response. Although Applicant appreciates the Examiner addressing Applicant's arguments, it appears the Examiner apparently fails to understand the points made in Applicant's previous Response. Accordingly, while Applicant incorporates by reference the arguments set forth in the April 4 Response, Applicant addresses the Examiner's arguments in the Final Office Action in turn below.

A. The Allocation Table Located in VRSM layer 101 is Not the Same "Memory" That is Includes Designated Blocks of Memory That Are Assigned and Accessed by Threads.

To clarify Applicant's position, claim 23 is presented below with emphasis to elements pertinent to Applicant's following remarks.

> 23. A system for assigning blocks of **memory**, the system comprising:
>
> **an area of memory** designated for coordinating the assignment of **the memory** to one or more threads requiring access to **the memory**, wherein the area including usage information reflecting usage of **the memory**; and
>
> a processor for performing a protocol for serializing access to **the memory** by the one or more threads based on the usage information, wherein the protocol allows a first thread to access **a first designated block of the memory** while another thread requests and secures access **to another block of the memory**.

Referring to the claim and the disclosure of *Snider*, Applicant asserts there are clear distinctions between the two.

For example, the "memory" recited in claim 23 is associated with various features of the claim. For instance, "an area of the memory" is designated for "coordinating assignment of the memory to one or more threads requiring access to the memory." In *Snider*, however, the allocation tables are located in VRSM 101, as acknowledged by the Examiner. VRSM 101 is a location used to manage access to a different memory, data structure 200, which corresponds to the heap of memory made up by memory 106 (*Snider*, 5:35-37.) Accordingly, *Snider* does not show the same "memory" including an area designated for coordinating the assigning of the same memory that is required access by one or more threads."

The Examiner asserts *Snider* teaches this recitation because, as asserted, the allocation table "which is part of the VRSM layer 101 is a memory location accessed by multiple threads." (OA at 9.) This assertion is incorrect for two reasons.

First, *Snider* does not teach threads that access VRSM layer 101 or its allocation tables. Instead, operating system 103 uses allocation functions to allocate memory from memory heap 106. (*Snider* at 3:33-35.) The Examiner asserts a processor is the same as a thread. (OA at 9, "only one processor or thread at a time can write access that memory.") In this regard, *Snider* does not show the processors 105 executing threads that access VRSM 101. Instead, as noted by the Examiner, processors 105 access "shared data structure 200," which corresponds to memory heap 106, and not VRSM 101 or its allocation tables.

Second, *Snider* merely discloses that operating system 103 may access VRSM layer 101 to perform allocation functions, a disclosure that does not teach or suggest the recitations of claim 23. For instance, claim 23 requires a protocol to allow "a first thread to access a first designated block of the memory while another thread requests and secures access to another block of the memory." Further, as noted above, the same "memory" must also include the "area" that is designated for coordinating the assignment of the memory to one or more threads. A proper review of *Snider* shows this is not the case in system 100. While operating system may access VRSM layer 101 to initiate allocation functions, these functions allocate memory from data structure 200 and memory heap 106, which are completely different memories. (*Snider* at 5:33-37.) This is a relevant distinction that should be given reconsideration by the Examiner because, as noted above, claim 23 recites the same "memory" including the "area" for designating and the designated areas for the first and second threads.

B. The Exclusive Write Capabilities of *Snider* Are Not The Same as Usage Information Recited in Claim 23.

The Examiner asserts because *Snider* allows only a single processor to write access the data structure 200, the reference discloses the usage information recited in claim 23. This position is misplaced for the following reasons.

First, claim 23 requires the "usage information" to be located in the same "area of memory designated for coordinating the assignment of the memory to one or more threads requiring access to the memory." *Snider*'s ability to block access to other processors while one access data structure 200 does not show usage information stored in the same area of memory designated for assignment of the memory, which according to the Examiner is the allocation tables in VRSM 101. That is, *Snider* does not teach, and the Examiner has not shown, "usage information" within the same area of memory that assigns the same memory to threads.

Second, claim 23 requires "a protocol for serializing access to the memory by the one or more threads *based on the usage information*. While *Snider* may allow serial access to the data structure or memory heap 106, Applicant's previous argument, which is restated, is *Snider* does not teach, and the Examiner has not shown, the serial access is based on "usage information" that is located in the same "area" of memory designated for "coordinating the assignment of the" same "memory to one or more threads."

C. The Asserted Combination of *Nikhil* and *Snider*

The Examiner asserts *Nikhil* "was used to provide evidence of the well known concept of allowing a first thread to access a designated block of memory while another thread requests and secures access to another block . . . ." (OA at 10.) In this regard, the Examiner argues that *Nikhil* shows the above recitations via its pipelining operations. However, *Snider* uses serial access techniques that block access to data structure 200 to more than one processor. (*Snider* at 7:1-5.) As noted by the Examiner, the pipelining features of *Nikhil*, on the other hand, are used to allow multiple operations to be processed without waiting for the completion of one operation to the next. Accordingly, one of ordinary skill in the art would find it counterproductive and non-motivating to implement an architecture that allows multiple operations to concurrently perform, as disclosed by *Nikhil*, with the serial access control system disclosed by *Snider*. Indeed, *Snider* teaches away from having multiple processors access data structure 200 at the same time to ensure the "integrity of the data." (*Snider* at 7:3-5.) Further, the system disclosed by *Nikhil* uses tokens to secure access to memory locations. This is a far cry from using VRSM layer 101 to control access to shared memory. In this regard, *Snider* is directed towards a centralized memory access control mechanism, whereas *Nikhil* uses distributed access control mechanisms via tokens. The Examiner points to no suggestion in the references that would have motivated one of ordinary skill in the art to look to *Nikhil* to modify *Snider*, as they are directed towards different and incompatible mechanisms.

D. The Examiner Does Not Properly Address the Arguments Set Forth by Applicant Regarding Dependent Claims 24-26

Claims 24-26 depend from claim 23. As explained, the cited art does not support the rejection of claim 23. As such, the cited art does not support the rejection of claims 24-26 for at least the same reasons set forth in connection with the response to the rejection of claim 23. As noted in the Response filed April 4, the cited art does not teach or suggest the recitations of these claims as asserted by the Examiner. For example, the Examiner admits that the cited art does not teach the size of the designated memory being determined by a user. Nonetheless, the Examiner asserts such recitations are obvious without providing an evidence supporting the assertion. (OA at 5.) As explained, conclusions of obviousness must be shown by substantial evidence. The Examiner has not pointed to any portion of the references that suggest the proposed combination. Instead, the Examiner presents an unsupported conclusion, such as alleging the proposed combination would allow the cited art to "serve [a] broader range of applications." These conclusions were not reached based on facts gleaned from the cited references. Accordingly, the Examiner has not established a *prima facie* case of obviousness with respect to claim 25, and thus, for this additional reason, the rejection of that claim under 35 U.S.C. § 103(a) should be withdrawn.

Further, the Examiner fails to address the recitations of claim 26. Nowhere does the Office Action address a designated block of memory being adjacent to a designated block of memory, as recited in claim 26. Indeed, the cited art fails to teach or suggest these recitations. For instance, *Snider* teaches a distributed memory system that creates a shared memory heap from separate memories 106. The reference does not suggest that the requested data structure is adjacent to another memory area associated with another thread's access to the memory. Further, *Nikhil et al.* fails to address blocks of memories in an allocation system, much less adjacent blocks of memory. Accordingly, because the Examiner fails to address the recitations of claim 26, and the cited art fails to teach or suggest them, Applicant submits the rejection to claim 26 is improper and should be withdrawn.

III. The Rejection of Claims 30-34

The Examiner maintains the same rejections of claims 30-34 under 35 U.S.C. § 103(a) over *Resman et al.* in view of *Nikhil et al.* set forth in the previous office action mailed January 26, 2005. The Examiner, however, supplements this rejection with comments addressing the arguments presented by Applicant in the April 4, 2005 Response. Although Applicant appreciates the Examiner addressing Applicant's arguments, the Examiner wrongly concludes the recitations of these claims are disclosed by the cited art. Accordingly, while Applicant incorporates by reference the arguments set forth in the April 4 Response (restated below), Applicant initially addresses the Examiner's lone response to Applicant's previous arguments regarding claims 30-34.

A. *Resman et al.* Does Not Teach Allocating, without Accessing an Operating System, a Block of Memory That Has a Size Designated by A User

The Examiner asserts *Resman et al.* teaches the above noted recitations of claim 30 in the Abstract, col. 2, lines 30-40, and col. 3, lines 6-8. These portions of *Resman et al.*, or any other portion, however, does not disclose or even suggest a user providing any input, much less designating the size of a memory. For example, col. 2, lines 30-36 of *Resman et al.* states,

> [a] data processing system includes an adaptive method for allocation of RAM as between procedures having both higher and lower priorities. The RAM is provided with first and second portions, the first portion for assignment to higher priority procedures and the second portion for assignment to lower priority procedures, higher priority procedures being able to access also the second portion of RAM. The adaptive method comprises the steps of: responding to a request for allocation of RAM to a higher priority procedure by determining if RAM is available from the first portion and, if not, allocating RAM from the second portion to the higher priority procedure.

Col. 3, lines 6-8 recite, "I/O control module 16 receives data from a host processor, converts it to a form suitable for storage and transmits it, via bus 18, to a RAM 20." Accordingly, it is clear *Resman et al.* does not teach or even suggest a user performing any designations. Indeed, the only reference to a user in the context of memory is found in col. 1, lines 65-66, which states, "[a]s an example, a printer has available to it a set amount of RAM depending upon the amount installed by the user." This statement merely shows a user may install a certain amount of RAM, but does not suggest designating a size of a block of memory that is allocated to a process without accessing an operating system.

As such, the Examiner's positions set forth in the Final Office Action are not supported by the cited art. Accordingly, Applicant requests the rejection of claim 30 under 35 U.S.C. § 103(a) be withdrawn, and the claim allowed. Further, because claims 31-34 depend from claim 30, these claims are also not supported by the cited art and should be allowed for at least the same reasons set forth above in connection with claim 30.

B. The Cited Art Does Not Teach or Suggest the Recitations of Claims 30-34, as Asserted by the Examiner

The Examiner asserts *Resman et al.* teaches allocating to a first process, without accessing an operating system, a first block of memory that has a size designated by a user, as recited in claim 30. In particular, the Examiner alleges that the allocation of a higher priority procedure (i.e., an application task) to a the AI/O RAM pool when the free RAM pool is full suggest the above recitations. The Examiner further asserts that *Resman et al.* teaches allocating to a second process, without accessing an operating system, a second block of memory that has a size designated by a user. Applicant disagrees with the Examiner's interpretation of *Resman et al.*

Resman et al. discloses a memory allocation system that allows applications to request and receive RAM space from a free RAM pool. If no space is available, an application is allowed access to a AI/O RAM pool. (*See Resman et al.*, col. 3, ll. 29-49.) I/O tasks are allocated space in an I/O fixed buffer pool. An I/O task may be allocated space in the AI/O RAM pool only when a certain amount of space is available in the free RAM pool. *Id.* at col. 3, ll. 50-62.

Contrary to the Examiner's assertions, *Resman et al.* does not teach or suggest allocating, without accessing an operating system, a first block of memory having a size designated by a user. The reference does not state that the size of any portion of the RAM pools are designated by a user. On the contrary, *Resman et al.* states that requests for RAM allocation are caused by an application running in CPU 14. (*See Resman et al.*, col. 3, ll. 29-30.) This software based allocation process does not provide for user input, much less input to designate a size of a block of memory to be allocated to a process. Further, the mere fact that *Resman et al.* allows an I/O task to access memory does (under certain conditions) does not bolster the Examiner's arguments. As explained, *Resman et al.* does not mention or disclose a user designated size of block of memory that is allocated without accessing an operating system to a first or second process.

The Examiner admits that *Resman et al.* does not teach allocating a second block of memory to the second process while the first process is accessing the first block of memory, as recited in claim 30. (OA at 6-7.) To make up for these deficiencies, the Examiner again refers to the instruction pipeline system of *Nikhil et al.* Applicant disagrees with the Examiner's interpretation of the cited art.

As explained, *Nikhil et al.* merely discloses an instruction pipeline process where tokens are used as identifiers to facilitate an instruction fetch and execution stage of a pipeline. Nowhere does the reference discuss controlling or allocating memory or portions of a memory in the manner recited in claim 30. Instead, the token queue disclosed by *Nikhil et al.* stores instruction identifiers that are used as references that assist in maintaining consistent processing within an instruction pipeline 36. Accordingly, contrary to the Examiner's assertions, *Nikhil et al.* does not teach or suggest allocating a second block of memory to the second process while the first process is accessing the first block of memory, as recited in claim 30.

Additionally, the requisite motivation to combine *Resman et al.* and *Nikhil et al.* is lacking. As explained, determinations of obviousness must be supported by evidence in the record. The Examiner again does not show that a skilled artisan considering *Resman et al.* and *Nikhil et al.*, and not having the benefit of Applicant's disclosure, would have been motivated to combine or modify the references in a manner resulting in the recitations of claim 30. In fact, the Examiner presents the same reasons for combining *Nikhil et al.* with *Resman et al.* as those set forth in the rejection of claim 23 in view of *Snider* and *Nikhil et al.* (*See Office Action*, p. 4, ll. 8-21 and p 6, l. 13 to p. 7, l. 10.) The Examiner's conclusion is not properly supported and does not show that a skilled artisan would have combined the references as alleged. The mere fact that *Nikhil et al.* mentions a pipeline process does not show that a skilled artisan would have been motivated to modify *Resman et al.* as alleged. Indeed, one of ordinary skill in the art would not have looked to an instruction level pipeline processing system, such as that taught by *Nikhil et al.,* for modifications to a memory allocation system within a printer processing system, such as that taught by *Resman et al.*

For at least these reasons, the Examiner has not established a *prima facie* case of obviousness with respect to claim 30, and thus, the rejection of that claim under 35 U.S.C. § 103(a) should be withdrawn and the claim allowed.

Claims 31-34 depend from claim 30. As explained, the cited art does not support the rejection of claim 30. As such, the cited art does not support the rejection of claims 31-34 for at least the same reasons set forth in connection with the response to the rejection of claim 30. Accordingly, Applicant requests that the rejection of these claims be withdrawn and the claims allowed.

IV. Conclusion

In view of the foregoing remarks, Applicant submits that this claimed invention, is neither anticipated nor rendered obvious in view of the cited art. Applicant therefore requests the Examiner's reconsideration and reexamination of the application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: October 11, 2005

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